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EXAMINER	
BELIVEAU, SCOTT E	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/239,907	Applicant(s) MACCORMACK ET AL.	
	Examiner Scott Beliveau	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 19 April 2004 have been fully considered but they are not persuasive with respect to claims 1, 3-12, 13-20, and 30-38.

With respect to applicant's arguments regarding the claim interpretation, the examiner respectfully disagrees. The elements reference by applicant are clearly designated and separate from the circuitry designated by the examiner in the grounds of rejection for the limitation of "circuitry for receiving the digital data stream". Furthermore, based on the applicant's interpretation of the claim, the arrangement of elements (ex. Figure 6) as supported in the specification would fail to provide adequate support for applicant's interpretation given that "memory" is similarly a part of the "circuitry for receiving the digital data stream".

With respect to the rejection of claims 1, 5, 10-11, 15, 20, 30-33, and 37-38 under Deiss, the examiner respectfully disagrees with applicant's interpretation of the rejection. As utilized in the grounds of rejection, "a memory" is cited as the combination of both the programmable SCID register [13] and the memory [18]. In conjunction with the decryption process, the reference teaches "if a match is detected the decoder communicates with the memory controller 17 and the smart card 31 to make the remainder of the entitlement payload available to the smart card (via the memory 18)" (Col 5, Lines 29-32). Accordingly, the "third control circuit" comprising the memory controller [17] outputs the particular memory address information associated with the stored entitlement encryption information,

so as to be accessed by the "second control circuit" comprising the smart card [31] and associated decryption information.

With respect to claims 6, 16, 17, and 34-36, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The particular existence of the MPEG-2 standard is both disclosed in the art of record and in applicant's admitted prior art (IA: Page 1, Lines 13-14). The Deiss reference clearly sets forth that the invention utilizes the MPEG standard, but does not disclose what particular flavor of the standard to utilize. Accordingly, a secondary reference was not supplied based on a reliance of knowledge generally available to one of ordinary skill in the art.

With respect to the rejection of claims 1, 3-11, and 13-20 under Dokic, as aforementioned, the examiner's interpretation of the claim is that the limitations are met given that the packet buffers within the digital signal processor [102] are physically separate from the receiving circuitry [112] as illustrated in Figure 3.

2. Applicant's arguments with respect to the rejection(s)of claim(s) 21-29 under Dokic in view of Blatter et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of a reinterpretation of combined Dokic and Blatter et al. references.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5, 10, 11, 15, 20, 30-33, 37, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Deiss (US Pat No. 5,521,979) (of record).

In consideration of claims 1 and 10, the Deiss et al. reference discloses a "receiver" or "set-top box" (Figure 3) that is operable to "demultiplex a digital data stream including data packets each having a packet identifier". The reference comprises a "input circuitry for receiving the digital data stream" [10/11], a "memory for storing packing identifiers corresponding to data packets required by the receiver and separate from the circuitry for receiving the digital data stream" [13/18], a "first control circuit for controlling the storage in the memory of the packet identifiers" [19] (Col 4, Lines 2-10), a "second control circuit for extracting a packet identifier from a data packet" [12/16/30/31], and a "third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory" [15/17]. Subsequently, in "response to a match", the memory controller "outputs the address in the memory responsive to a match" wherein the "second control circuit . . . retrieves control information associated with the packet identifier" associated with encryption information and subsequently "demultiplexes the input data packet responsive to the match signal" (Col 4, Lines 40-67; Col 5, Lines 30-33).

Claims 11 and 20 are rejected in view of the rejection of claim 1. The "method of demultiplexing a digital data stream" in conjunction with a "set-top-box" is met wherein the reference teaches the following steps: "inputting the digital data stream" (Col 3, Lines 19-25), "storing . . . all packet identifiers. . . required by the receiver" (Col 3, Line 50 – Col 4, Line 10), and "determining", "extracting", and "demultiplexing" under the control of a "second" and "third control circuit" packets responsive to a "match" (Col 4, Lines 40-67; Col 5, Lines 30-33).

Claims 5 and 15 are rejected wherein the "responsive to the match signal not being set, the second control circuit discards the input packet" (Col 3, Lines 60-65).

In consideration of claims 30 and 38, the Deiss et al. reference discloses a "receiver" or "set-top box" (Figure 3) that is operable to "demultiplex a digital data stream including data packets each having a packet identifier". The embodiment comprises a "first data structure" [18], a "second data structure" [13/17], a "first control circuit" [12/17/30/31], and a "second control circuit" [15]. In operation, the embodiment implements a method wherein "packet identifiers" from an "inputted" digital data stream [10/11] are extracted "under the control of a first control circuit" [12]. A "second control circuit" [15] "determines" whether the extracted packet identifier matches one of the packet identifiers in the "second data structure" [13/17] and "sets a match signal" responsive to a match. Subsequently "addressing information" is "outputted" and "control information from the first data structure" associated with the decryption of the payload is "retrieved" and "under the control of the first control circuit" [12/17/30/31] the input data packet is "demultiplexed" (Col 3, Line 66 – Col 4, Line 55).

Claims 31 and 32 are rejected wherein "under the control of the first control circuit" [12/17/30/31], the input data packet is "processed" and "transferred . . . to a destination address identified by the retrieved control information" (Col 4, Lines 11-46).

Claim 33 is rejected wherein the "responsive to the match signal not being set, the second control circuit discards the input packet" (Col 3, Lines 60-65).

Claim 37 is rejected wherein the step of determining a match comprises "systematically searching the second data structure" in conjunction with the cycling through memory locations within the register for the data (Col 8, Lines 17-52).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 6, 16-17, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deiss (US Pat No. 5,521,979) in view of applicant's admitted art.

In consideration of claims 6, 16-17, and 34-35, the embodiment discloses that the "digital data stream" may be an "MPEG" encoded stream, but does not explicitly disclose what form of MPEG encoding is used. Applicant's admitted prior art discloses the existence of the MPEG-2 standard (IA: Page 1, Lines 13-14).Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize "MPEG-2" encoding for the purpose of using a standard encoding scheme in which digital television signals or HDTV signals utilize. The MPEG-2 standard defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets.

In consideration of claim 36, the embodiment comprises "filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver" (Col 3, Line 38 – Col 4, Line 10).

8. Claims 1, 3-11, 13-20, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic et al. (US Pat No. 5,959,659), in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer.

In consideration of claims 1 and 10, the examiner refers the applicant to Figures 3 and 5, the Dokic et al. reference, which discloses a decoder that may function as a "set top box" or "receiver for the demultiplexing digital data streams . . . including data packets having a packet identifier" such as those defined by the MPEG-2 specification (Col 1, Lines 19-23; Col 2, Lines 45-65). The aforementioned Dokic et al. reference reads on the claimed language in view of Figures 3 and 5. Figure 3 illustrates a block diagram of the "receiver"

architecture comprising: "circuitry for receiving the digital data stream" [112] (Col 6, Lines 10-12), a demultiplexing section [104], and a control section [108] (Col 5, Lines 60-67 – Col 6, Lines 1-9). Referring now to Figure 5, the demultiplexing section is further shown to comprise "a memory for storing packet identifiers that correspond to data packets required by the receiver" [205] (Col 8, Lines 26-31) that is "separate from the circuitry for receiving the digital data stream" (Figure 3), "a first control circuit" or host microprocessor [106], and a "second" and "third control circuit" embodied via the controller [204] of the digital signal processor [102]. The "first control circuit" provides "packet identifiers of data packets required by the receiver" to the "memory" [205] (Col 8, Lines 28-31, 58-60; Col 9, Lines 10-23). The "second control circuit" extracts the payloads of the transport packets including "control information" responsive to a "match signal" as indicated by the "third control circuit" (Col 8, Lines 20-52; Col 9, Lines 18-43).

As to the limitation pertaining to the "control information", the claimed language is not limiting other than to require that the "control information" is something that is "associated with the packet identifier". The Dokic reference teaches that the MPEG-2 transport stream may comprise packets of "control information" such as the program map table (PMT) or program association table (PAT) from the MPEG-2 transport stream (Col 4, Lines 22-27). These program specific information (PSI) tables are associated with reserved packet identifiers (PID) (ISO/IEC 13818-1: Section 2.4.4). As such, the Dokic et al. reference teaches that the PID from the received packet is parsed from the transport packet to identify the type of data carried by the transport packet. Accordingly, "control information" may be

temporarily stored in the packet buffers [200/202] prior to being transferred to the host processor [106] (Col 9, Lines 29-43).

Alternatively, it is further noted that the packet header may further comprise "control information" in the form of timing information (PCR) used in the decoding of the payload. The packet buffers [200/202] or "memory" are disclosed to store the entire transport packet comprising "control information associated with the packet identifier" (Col 7, Lines 66-67 – Col 8, Lines 1-4). The Dokic reference goes on to suggest that either the "entire packet" or the payload may be forwarded from the "memory" (Col 9, Lines 39-43). The claim language is subsequently not limiting such that the "entire packet" comprising both the identifier and the "control information associated with the identifier" contained within the packet header may be "accessed" and "demultiplexed".

With respect to the limitation pertaining to "outputting an address", the Dokic reference does not explicitly disclose nor preclude details pertaining to the retrieval of information through a "memory address". The reference explicitly discloses that the preferred embodiment of the digital signal processor is a DSP2111 manufactured by Analog Devices® (Col 7, Lines 53-55). The ADSP-2100 Family User's Manual – Chapter 4 describes that the circular buffers rely on "addresses" in order to determine where to locate the next piece of information in a circular buffer may be located (Sections 4.2.3 – 4.3.2). Accordingly, it would have obvious to one of ordinary skill at the time of the invention to utilize the teachings of the ADSP-2100 User's Manual such that the embodiment would implicitly "output an address in the memory responsive to a match" in order to know where in the on-board memory [200/202/205] to retrieve the "entire packet" comprising both the identifier

and "control information" for the purposes of implementing the preferred embodiment using components explicitly disclosed by Dokic.

Claims 11 and 20 are rejected in view of the rejection of claim 1. The "method of demultiplexing a digital data stream" in conjunction with a "set-top-box" is met wherein the reference teaches the following steps: "inputting the digital data stream" (Figure 3; Col 5, Lines 60-67 – Col 6, Lines 1-9), "storing . . . all packet identifiers. . . required by the receiver" (Col 8, Lines 28-31, 58-60; Col 9, Lines 10-23), and "determining", "extracting", and "demultiplexing" under the control of a "second" and "third control circuit" packets responsive to a "match" (Col 8, Lines 20-52; Col 9, Lines 18-43).

Claims 3, 4, 13, and 14 are rejected in view of Figure 5 wherein "the second control circuit" [204] controls the transfer of and/or processes "the input data packet to a destination" such as data buffers [206/208/210] or host microprocessor as "identified by the control information" (Col 8, Lines 31-37, 53-67). It is taught that should the "input data packets" contain private data, the entire packet will either be "transferred". Alternatively, the packet may be "processed" such that only the payload data is "transferred" (Col 9, Lines 39-53).

Claims 5 and 15 are rejected wherein the Dokic reference teaches that the packet is "discarded" if a "match" is not found (Col 8, Lines 51-52)

Claims 6, 7, 16, and 17 are rejected wherein the reference teaches a method/apparatus for the interpretation and demultiplexing of received MPEG-2 transport packets (Col 7, Lines 49-59). The MPEG-2 standard (incorporated by reference) defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets. The instant application further supports this definition (Page 2, Lines 5-8).

In consideration of claims 8 and 18, the component elements of the "input" data stream are well known in the art, as evidenced by the MPEG-2 specification,. Figures 1-2 of the Dokic reference illustrates that the "input data packet comprises program specific information" or PSI tables (Col 2, Lines 3-19). As aforementioned, the receiver uses these PSI tables to derive PIDs that corresponds to desired programming which are subsequently used by the "second control circuit" [204] to "retain only those data packets having sections required by the receiver" (Col 2, Lines 29-44; Col 8, Lines 20-31, 48-52).

Claim 9 is rejected wherein the "first control circuit" is a "receiver processor" [106] which controls the overall operation of the "receiver" (Col 13, Lines 13-32). The "second" and "third control circuits" [204] are embedded within a digital signal processor [106] that is coupled to a PAL [118]. The digital signal processor [106] functions as both a "search engine" to identify buffered packets and a "transport processor" to move the packets into the appropriate buffer as aforementioned (Col 8, Lines 20-52).

Claim 19 is rejected wherein the "third control circuit" [204] "systematically" searches the transport packet buffers [200/202] for a "match". Figures 6A-C further illustrate a "systematic" method for "searching the memory" in conjunction with the demultiplexing process.

Claim 37 is rejected wherein the "first" and "second control circuits" [204] are embedded within a digital signal processor [106] that is coupled to a PAL [118]. Accordingly, the digital signal processor [106] functions as both a "search engine" to identify buffered packets and a "transport processor" to move the packets into the appropriate buffer as aforementioned (Dokic et al.: Col 8, Lines 20-52).

9. Claims 21-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic et al. (US Pat No. 5,959,659), in view of Blatter et al. (US Pat No. 5,844,595).

In consideration of claims 21 and 29, as aforementioned, the Dokic et al. reference discloses a decoder that may function as a "set top box" or "receiver for the demultiplexing digital data streams . . . including data packets having a packet identifier" such as those defined by the MPEG-2 specification (Col 1, Lines 19-23; Col 2, Lines 45-65). Figure 3 illustrates a block diagram of the "receiver" architecture comprising: "input circuitry for receiving the digital data stream" [112] (Col 6, Lines 10-12), a demultiplexing section [104], and a control section [108] (Col 5, Lines 60-67 – Col 6, Lines 1-9). The demultiplexing section, as illustrated in Figure 5 comprises a data structure [205] for storing packet identifiers that correspond to data packets required by the receiver (Col 8, Lines 26-31) and a "first" and "second control circuits" [204] of the digital signal processor [102] for "extracting a packet identifier from a data packet in the digital data stream input", "determining whether such matches one of the packet identifiers in the first data structure", and "responsive to a match" is operable to "demultiplex the input data packet" (Col 8, Lines 20-52; Col 9, Lines 18-43).

The reference, however, does not explicitly disclose nor preclude the particulars pertaining to the "first" and "second data structure" as particularly claimed nor does it disclose the particular usage of encryption/decryption in conjunction with the MPEG-2 transport as is understood in the art. The Blatter et al. reference discloses the usage of encryption/decryption in conjunction with a MPEG demultiplexor comprising a "first" [45] and "second data structure" [45] wherein the "control information" or decryption information

associated with the "second data structure" [45] is memory mapped or "accessed based on addressing information extracted from the first data structure" (Col 4, Line 56 – Col 5, Line 19). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the data structure [205] of Dokic et al. reference to comprise a "first" and "second data structure" such as those employed by Blatter et al. such that "responsive to a match" the "addressing information" associated with the "control information" is "outputted" and "retrieved" for the purpose of advantageously providing a means to employ encryption/decryption in conjunction with transmitted MPEG video and to further provide a low-overhead mechanism by which processes can synchronize and communicate by reducing reduce I/O data movement.

Claims 30 and 38 are rejected in view of the rejection of claims 21 and 29. The "method of demultiplexing a digital data stream" in conjunction with a "set-top-box" is met wherein the reference teaches the following steps: "inputting the digital data stream" (Dokic et al.: Figure 3; Col 5, Lines 60-67 – Col 6, Lines 1-9), "storing . . . packet identifiers required by the receiver in a second data structure" [205] (Col 8, Lines 28-31, 58-60; Col 9, Lines 10-23), and "determining", "extracting", and "demultiplexing" under the control of a "second" and "third control circuit" packets responsive to a "match" (Dokic et al.: Col 8, Lines 20-52; Col 9, Lines 18-43). As aforementioned, the Dokic reference does not explicitly disclose the particular usage of "outputting addressing information" in conjunction with a "first" and "second data structure". The Blatter et al. reference discloses the usage of a "first" [45] and a "second" data structure" [45] whereupon addressing information from the "second data structure" [45] may be utilized to access "control information" associated with the decryption

of packets from the "first data structure" [45]. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dokic et al. reference to further employ a "first" and "second data structure" that employs memory mapping techniques such as those employed by Blatter et al. for the purpose of advantageously providing a means to employ encryption/decryption in conjunction with transmitted MPEG video and to further provide a low-overhead mechanism by which processes can synchronize and communicate by reducing reduce I/O data movement.

In consideration of claims 22-23 and 31-32, the Blatter et al. reference further discloses that the "control information" further identifies "destination address information" (Col 5, Lines 5-8). Accordingly, "the second control circuit" [204] controls the transfer of and/or processes "the input data packet to a destination" such as data buffers [206/208/210] or host microprocessor as "identified by the control information" (Dokic et al.: Col 8, Lines 31-37, 53-67).

Claims 24 and 33 are rejected wherein the Dokic reference teaches that the packet is "discarded" if a "match" is not found (Col 8, Lines 51-52)

Claims 25-26 and 34-35 are rejected wherein the reference teaches a method/apparatus for the interpretation and demultiplexing of received MPEG-2 transport packets (Col 7, Lines 49-59). The MPEG-2 standard (incorporated by reference) defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets. The instant application further supports this definition (Page 2, Lines 5-8).

In consideration of claims 27 and 36, the component elements of the "input" data stream are well known in the art, as evidenced by the MPEG-2 specification,. Figures 1-2 of the

Dokic reference illustrates that the "input data packet comprises program specific information" or PSI tables (Col 2, Lines 3-19). As aforementioned, the receiver uses these PSI tables to derive PIDs that corresponds to desired programming which are subsequently used by the "second control circuit" [204] to "retain only those data packets having sections required by the receiver" (Dokic et al.: Col 2, Lines 29-44; Col 8, Lines 20-31, 48-52).

Claims 28 and 37 are rejected wherein the "first" and "second control circuits" [204] are embedded within a digital signal processor [106] that is coupled to a PAL [118]. Accordingly, the digital signal processor [106] functions as both a "search engine" to identify buffered packets and a "transport processor" to move the packets into the appropriate buffer as aforementioned (Dokic et al.: Col 8, Lines 20-52).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Beliveau whose telephone number is 703-305-4907. The examiner can normally be reached on Monday-Friday from 8:30 a.m. - 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on 703-305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SEB
July 9, 2004

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